REMARKS

The Office Action dated December 14, 2005, has been received and carefully considered. In this response, claims 1, 21, 60, and 101-107 have been amended. Entry of the amendments to claims 1, 21, 60, and 101-107 is respectfully requested. Reconsideration of the outstanding objections/rejections in the present application is also respectfully requested based on the following remarks.

I. THE OBJECTION TO CLAIMS 59 AND 60

On page 2 of the Office Action, claims 59 and 60 were objected to under 37 CFR § 1.75(c) as being of improper antecedent form. This objection is hereby respectfully traversed with amendment.

Claim 60 has been amended to provide proper antecedent basis.

In view of the foregoing, it is respectfully requested that the aforementioned objection to claims 59 and 60 be withdrawn.

II. THE INDEFINITENESS REJECTION OF CLAIMS 21 AND 102

On pages 2-3 of the Office Action, claims 21 and 102 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly

claim the invention. This rejection is hereby respectfully traversed with amendment.

Claims 21 and 102 have been amended to provide proper antecedent basis.

In view of the foregoing, it is respectfully requested that the aforementioned indefiniteness rejection of claims 21 and 102 be withdrawn.

III. THE PROVISIONAL DOUBLE PATENTING OBJECTION

On page 3 of the Office Action, claims 103 and 106 and claims 104 and 107 were provisionally objected to under 37 CFR § 1.75(c) as being substantial duplicates of each other. This objection is hereby respectfully traversed with amendment.

Claims 102-104, 106, and 107 have been amended to provide proper antecedent basis and thereby render the above-mentioned objection moot.

In view of the foregoing, it is respectfully requested that the aforementioned double patenting objection of claims 103 and 106 and claims 104 and 107 be withdrawn.

IV. THE ANTICIPATION REJECTION OF CLAIMS 1-23, 28, 30-44, 46, 47, 52, 62-68, 76-84, 86, 92, 93, 98, 100-103, 105, AND 106

On pages 4-13 of the Office Action, claims 1-23, 28, 30-44, 46, 47, 52, 62-68, 76-84, 86, 92, 93, 98, 100-103, 105, and 106

were rejected under 35 U.S.C. § 102(e) as being anticipated by Roohparvar (U.S. Patent Application Publication No. US2005/0259506). This rejection is hereby respectfully traversed.

Regarding claim 1, the Examiner asserts that Roohparvar teaches a method for scheduling a device command comprising: issuing a first device command (i.e., a READ command); and issuing a first value (i.e., m clocks), wherein the first value determines, at least in part, a first performance time at which the first device command is to be performed (see paragraph [0077] and Figure 3). However, it is respectfully submitted that Roohparvar fails to teach, or even suggest, such a method. Instead, Roohparvar merely teaches that a mode register (148) stores bits representing a Column Address Strobe (CAS) latency delay (i.e., m clocks) between the registration of a READ command and the availability of read data on output lines of a memory device (see paragraphs [0066] and [0077], and Figures 1 and 3). This teaching by Roohparvar does not teach, or even suggest, the presently claimed invention for at least the following reasons.

First, Roohparvar does not teach, or even suggest, issuing a first value associated with the first device command, as presently claimed. Specifically, the Examiner asserts that

Roohparvar teaches issuing a first value associated with the first device command by disclosing that a mode register (148) stores bits representing a CAS latency delay (i.e., m clocks) between the registration of a READ command and the availability of read data on output lines of a memory device. However, Roohparvar does not teach, or even suggest, that these "m clock" bits are associated with a specific command (e.g., a first device command). In contrast, the "m clock" bits as disclosed by Roohparvar represent the CAS latency delay for all READ commands. Claim 1 has been amended to make this feature more clear to the Examiner. Thus, Roohparvar does not teach, or even suggest, issuing a first value associated with the first device command, as presently claimed.

Second, Roohparvar does not teach, or even suggest, issuing a first value associated with the first device command, as presently claimed. Specifically, the Examiner asserts that Roohparvar teaches issuing a first value associated with the first device command by disclosing that a mode register (148) stores bits representing a CAS latency delay (i.e., m clocks) between the registration of a READ command and the availability of read data on output lines of a memory device. However, Roohparvar does not teach, or even suggest, that these "m clock" bits are issued associated with the READ command. Indeed,

Roohparvar does not teach, or even suggest, that these "m clock" bits are issued in any manner. Thus, Roohparvar does not teach, or even suggest, issuing a first value associated with the first device command, as presently claimed.

Third, Roohparvar does not teach, or even suggest, issuing a first value associated with the first device command, wherein the first value determines, at least in part, a first performance time at which the first device command is to be performed, as presently claimed. Specifically, the Examiner asserts that Roohparvar somehow teaches that the first value determines, at least in part, a first performance time at which the first device command is to be performed by disclosing that a mode register (148) stores bits representing a CAS latency delay (i.e., m clocks) between the registration of a READ command and the availability of read data on output lines of a memory device. However, Roohparvar does not teach, or even suggest, that these "m clock" bits determine, at least in part, a time at which the READ command is performed. In contrast, the "m clock" bits as disclosed by Roohparvar merely represent the CAS latency delay between the registration of a READ command and the availability of read data on output lines of a memory device. Indeed, the READ command as disclosed by Roohparvar is performed as soon as it is registered. That is, it is only the

availability of read data on output lines of the memory device that is delayed by the latency represented by the "m clock" bits, not the performance of the READ command. Thus, Roohparvar does not teach, or even suggest, issuing a first value associated with the first device command, wherein the first value determines, at least in part, a first performance time at which the first device command is to be performed, as presently claimed.

In view of the foregoing, it is respectfully submitted that Roohparvar does not teach, or even suggest, the claimed invention as recited in claim 1. Accordingly, it is respectfully submitted that claim 1 should be allowable over Roohparvar.

Claims 2-23, 28, 30-44, 46, 47, 52, 62, and 63 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-23, 28, 30-44, 46, 47, 52, 62, and 63 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

Regarding claim 64, the Examiner asserts that Roohparvar teaches a controller (i.e., 340 in Figure 32) for scheduling

commands comprising a driver for issuing commands and associated non-zero delay values to at least one device (i.e., 350 in Figure 32) coupled to the controller, wherein a first delay value (i.e., m clocks) is associated with a first performance time at which a first command (i.e., the READ command) of the commands is to be performed by the device (see paragraph [0077] and Figures 3 and 32). However, for similar reasons as set forth above with respect to claim 1, it is respectfully submitted that Roohparvar fails to teach, or even suggest, such a controller. Accordingly, it is respectfully submitted that claim 64 should be allowable over Roohparvar.

Claims 65-68 and 76-78 are dependent upon independent claim 64. Thus, since independent claim 64 should be allowable as discussed above, claims 65-68 and 76-78 should also be allowable at least by virtue of their dependency on independent claim 64. Moreover, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

Regarding claim 79, the Examiner asserts that Roohparvar teaches a device comprising: a receiver (i.e., the command register in Figure 1A) for receiving a first device command (i.e., the READ command), a first value (i.e., m clocks) associated with the first device command, wherein a first

performance time is associated with the first value; means for performing the first device command at the first performance time; and control circuitry for controlling the means to cause the means to perform the first device command at the first performance time (see paragraph [0077] and Figures 1A and 3). However, for similar reasons as set forth above with respect to claim 1, it is respectfully submitted that Roohparvar fails to teach, or even suggest, such a device. Accordingly, it is respectfully submitted that claim 79 should be allowable over Roohparvar.

Claims 80-84, 86, 92, 93, 98, and 100 are dependent upon independent claim 79. Thus, since independent claim 79 should be allowable as discussed above, claims 80-84, 86, 92, 93, 98, and 100 should also be allowable at least by virtue of their dependency on independent claim 79. Moreover, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

Regarding claim 101, the Examiner asserts that Roohparvar teaches a system comprising: a first device (i.e., the command register in Figure 1A) configured to issue commands (i.e., READ commands) and values (i.e., delay values), wherein each of the values is associated with a respective one of the commands; and

a second device (i.e., the command register in Figure 1A) configured to receive the commands (i.e., READ commands) and the associated values (i.e., delay values), the second device further configured to execute each command at a time determined at least in part by the value associated with the command; wherein the first device is further configured to dynamically determine the value associated with at least one of the commands (see paragraph [0077] and Figures 1A and 3). However, for similar reasons as set forth above with respect to claim 1 (and in view of the fact that the Examiner incorrectly asserts that Roohparvar teaches that the command register in Figure 1A both issues and receives commands), it is respectfully submitted that Roohparvar fails to teach, or even suggest, such a system. Accordingly, it is respectfully submitted that claim 101 should be allowable over Roohparvar.

Claims 102 and 103 are dependent upon independent claim 101. Thus, since independent claim 101 should be allowable as discussed above, claims 102 and 103 should also be allowable at least by virtue of their dependency on independent claim 101. Moreover, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

Regarding claim 105, the Examiner asserts that Roohparvar teaches a system comprising: a first device (i.e., the command register in Figure 1A) comprising: means for issuing commands (i.e., READ commands); and means for issuing values (i.e., delay values), wherein each of the values is associated with a respective one of the commands; and a second device (i.e., the command register in Figure 1A) comprising: means for receiving commands (i.e., READ commands); means for receiving the associated values (i.e., delay values); and means for performing each of said commands at a time determined at least in part by the associated value (see paragraph [0077] and Figures 1A and 3). However, for similar reasons as set forth above with respect to claim 1 (and in view of the fact that the Examiner incorrectly asserts that Roohparvar teaches that the command register in Figure 1A both issues and receives commands), it is respectfully submitted that Roohparvar fails to teach, or even suggest, such a system. Accordingly, it is respectfully submitted that claim 105 should be allowable over Roohparvar.

Claim 106 is dependent upon independent claim 105. Thus, since independent claim 105 should be allowable as discussed above, claim 106 should also be allowable at least by virtue of its dependency on independent claim 105. Moreover, this claim recites additional features which are not disclosed, or even

suggested, by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1-23, 28, 30-44, 46, 47, 52, 62-68, 76-84, 86, 92, 93, 98, 100-103, 105, and 106 be withdrawn.

V. THE OBVIOUSNESS REJECTION OF CLAIMS 24-27, 29, 48-51, 53, 59, 60, 69-75, 94-97, AND 99

On pages 14-15 of the Office Action, claims 24-27, 29, 48-51, 53, 59, 60, 69-75, 94-97, and 99 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Roohparvar (U.S. Patent Application Publication No. US2005/0259506). This rejection is hereby respectfully traversed.

Claims 24-27, 29, 48-51, 53, 59, 60, 69-75, 94-97, and 99 are dependent upon independent claims 1, 64, and 79. Thus, since independent claims 1, 64, and 79 should be allowable as discussed above, claims 24-27, 29, 48-51, 53, 59, 60, 69-75, 94-97, and 99 should also be allowable at least by virtue of their dependency on independent claims 1, 64, and 79. Moreover, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 24-27, 29, 48-51, 53, 59, 60, 69-75, 94-97, and 99 be withdrawn.

VI. THE OBVIOUSNESS REJECTION OF CLAIMS 45, 54-58, 61, 85, 87-91, 104, AND 107

On pages 15-17 of the Office Action, claims 45, 54-58, 61, 85, 87-91, 104 and 107 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Roohparvar (U.S. Patent Application Publication No. US2005/0259506) in view of Cashion et al. (U.S. Patent No. 6,195,434). This rejection is hereby respectfully traversed.

Claims 45, 54-58, 61, 85, 87-91, 104 and 107 are dependent upon independent claims 1, 79, 101, and 105. Thus, since independent claims 1, 79, 101, and 105 should be allowable as discussed above, claims 45, 54-58, 61, 85, 87-91, 104 and 107 should also be allowable at least by virtue of their dependency on independent claims 1, 79, 101, and 105. Moreover, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 45, 54-58, 61, 85, 87-91, 104 and 107 be withdrawn.

VII. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

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